Nanoscale Technology Research and Development: what are the challenges ahead?

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Abstract:

After receiving his Ph.D. degree in Electrical Engineering for his dissertation on nanoscale Strained-Silicon electron devices from MIT in 2003, Dr. Nayfeh joined IBM SRDC, where he is currently senior engineer with responsibility for technology research and development. Dr. Nayfeh's nanoscale device design work has resulted in the successful deployment of 65 and 45-nm technology-nodes, enabling integrated chips (ICs) that are more powerful compared to prior technologies due to increased circuit functionality measured as the product of speed and density at fixed power density. Such ICs are found in commercial products including the IBM system p and z server machines, and Nintendo Wii, Sony PlayStation, and Microsoft X-Box game consoles.

In this talk, I will discuss the challenges involved to continue with successful technology deployment of future nodes, as 9-nm technology will be reaching market towards the end of this decade, in order to satisfy consumer demand for faster performance and lower power electronic products, and how universities/research institutions, in this region can contribute technically to this challenge from the experimental, theoretical and student training perspectives. Considerable innovation, covering the fields of electrical engineering, materials science, chemistry, and physics, will be required to support such small nanoscale dimensions. Already, power dissipation for an IC is roughly equal to that of a light bulb (200 W/cm2), and as devices are scaled further, this density is expected to increase further, due to physical limits on scaling that are almost impossible to break due to quantum mechanical tunneling leakage and reliability requirements, such as the gate insulator thickness which is near the limit of 1-nm which is only a few monolayers of atoms. Furthermore, since the minimum contacted pitch that is projected for the 9-nm technology node is only 50-nm, aggressive scaling of the gate length down to around 10-nm is required simply in order to have sufficient space to integrate the electrical contacts. This is an extremely difficult integration challenge due to such tight space, and a difficult physics problem due to high leakage in such 10-nm devices. Furthermore, the transport physics at such small dimensions will

require more advanced modeling that includes quantum mechanical scattering effects in order to predict the drive current in such devices accurately. There are several paths under investigation for reducing power density, but I will focus on two that are promising, and they are: (1) moving from a planar to a non-planar design structure, and (2) heterogenous integration of novel channel materials with Silicon. The non-planar design results in less leakage due to improved gate control over the charged carriers, allowing for shorter gate lengths helping to satisfy the space/density requirement. The novel channel materials, allow for aggressive reduction of the power supply voltage without performance loss due to amazingly higher mobility of the carriers over Silicon. Materials that are under investigation include: III-V compound semiconductors, and Carbon allotropes at low quantum mechanical confinement dimensions, specifically 2-D sheet of monolayer Graphene and single-walled Carbon nanotube wires.